REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R234-94	94-07-14	Monica L. Poelking
B	Add devices types 03-04. Add case outlines N, Y. Editorial changes throughout.	96-09-03	Monica L. Poelking

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32		

REV STATUS OF SHEETS																
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Christopher A. Rauch

CHECKED BY
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APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
92-10-07

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, CHMOS SINGLE-CHIP, 8-BIT MICROCONTROLLER WITH 32K BYTES OF EPROM PROGRAM MEMORY, MONOLITHIC SILICON

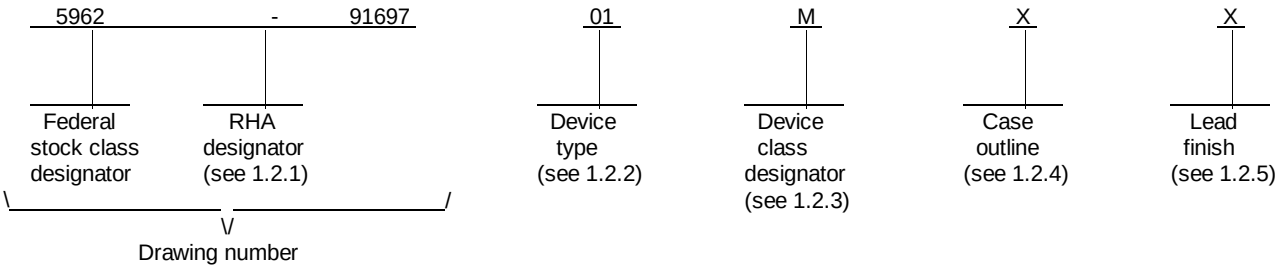
SIZE	CAGE CODE	
A	**67268**	**5962-91697**

SHEET 1 OF 32

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device classes M and Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	87C51FC	High performance CHMOS single chip 8-bit microcontroller with 32K bytes user programmable EPROM
02	87C51FC-16	High performance CHMOS single-chip 8-bit microcontroller with 32K bytes user programmable EPROM
03	87C51FC	High performance CHMOS single chip 8-bit microcontroller with 32K bytes user programmable EPROM
04	87C51FC-16	High performance CHMOS single-chip 8-bit microcontroller with 32K bytes user programmable EPROM

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment 1/
Q or V	Certification and qualification to MIL-PRF-38535

1/ Any device outside the traditional performance environment; i.e., an operating temperature range of -55°C to +125°C and which requires hermetic packaging.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	GQCC1-J44	44	Ceramic chip carrier, J-leaded package 2/
T	See figure 1	44	Ceramic chip carrier, J-leaded package 2/
U	CQCC1-N44	44	Square chip carrier package 2/
X	CDIP2-T40 or GDIP1-T40	40	Dual-in-line package 2/
Z	See figure 1	44	Ceramic chip carrier, gullwing-leaded package 2/
Y	MS-018-AC 3/	44	Plastic chip carrier, J-leaded
N	MS-011-AC 3/	40	Plastic dual-in-line package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 4/

Storage temperature range . . . . . -65° C to +150° C
Voltage on EA/V_{PP} pin to V_{SS} . . . . . 0.0 V dc to +13.0 V dc
Voltage on any other pin to V_{SS} . . . . . -0.5 V dc to +6.5 V dc
Maximum I_{OL} per I/O pin . . . . . 15 mA
Power dissipation (P_D) . . . . . 1.5 W 5/
Lead temperature (soldering 10 seconds) . . . . . 265° C
Thermal resistance, junction-to-case (Θ_{JC}):
  Cases U, X and M . . . . . See MIL-STD-1835
  Cases T, Z and N . . . . . 14° C/W
  Cases Y . . . . . 15° C/W
Endurance . . . . . 50 cycles/byte, minimum
Data retention . . . . . 10 years, minimum

1.4 Recommended operating conditions.

Case Operating Temperature Range
  devices 01, 02 . . . . . -55° C to +125° C 6/
  devices 03, 04 . . . . . -40° C to +85° C 6/
Supply Voltage, Vcc . . . . . +5.0 V dc ± 20%
Oscillator frequency . . . . . 3.5 MHz to 16 MHz

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) . . . . . XX percent 7/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION
MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS
MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ See JEDEC Publication 95
4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
5/ Power dissipation based on package heat transfer limitations, not device power consumption.
6/ Case temperatures are instant on.
7/ Values will be added when they become available.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publication. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the sloicitaion. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices.

(Applications for copies should be addressed to the Electronic Industry Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

3.11 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.11.2 Programmability of EPROMS. When specified, devices shall be programmed in accordance with the specified pattern using the procedures and characteristics specified in 4.6 herein and table III.

3.11.3 Verification and erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern using the procedures and characteristics specified in 4.6 and table III, or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All	-0.5 2/	$0.2\ V_{CC}$ -0.1	V
Input high voltage (except XTAL1, RST)	V_{IH}				$0.2\ V_{CC}$ +0.9	V_{CC}+0.5 2/	
Input high voltage (XTAL and RST)	V_{IH1}				$0.7\ V_{CC}$	V_{CC}+0.5 2/	
Output low voltage (ports 1,2,3) 3/	V_{OL}	I_{OL} = 100 µA 4/ I_{OL} = 1.6 mA I_{OL} = 3.5 mA				0.3 0.45 1.0	
Output low voltage (port 0, ALE, PSEN) 3/	V_{OL1}	I_{OL} = 200 µA 4/ I_{OL} = 3.2 mA I_{OL} = 7.0 mA				0.3 0.45 1.0	
Output high voltage (port 1, 2, 3, ALE, PSEN)	V_{OH}	I_{OH} = -10 µA I_{OH} = -30 mA I_{OH} = -60 mA			V_{CC}-0.3 V V_{CC}-0.7 V V_{CC}-1.5 V		
Output high voltage (ports 0, in external bus mode)	V_{OH1}	I_{OH} = -200 µA 5/ I_{OH} = -3.2 mA I_{OH} = -7.0 mA				V_{CC}-0.3 V V_{CC}-0.7 V V_{CC}-1.5 V	
Logical 0 input current (ports 1, 2, and 3)	I_{IL}	V_{IN} = 0.45 V				-75	µA
Input leakage current (port 0)	I_{IL}	$0.45 \le V_{IN} \le V_{CC}$				±10	
Logical 1 to 0 transition current (ports 1, 2, and 3)	I_{TL}	V_{IN} = 2.0 V				-750	
RST pulldown resistor	R_{RST}				40	225	kΩ
Power supply current Running at 16 MHz Idle mode at 16 Mhz Power down mode	I_{CC}	6/ 7/	1,2,3			 45 15 130	 mA mA µA
Pin capacitance 2/	C_{IO}	at 1.0 MHz, 25°C See 4.4.1c	4	All		10	pF
Functional testing		See 4.4.1e, V_{CC} = 4.0 V	7,8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.0\ V \le V_{CC} \le 6.0\ V$ $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ALE pulse width	t_{LHLL}	Load capacitance for port 0, ALE/PROG and PSEN = 100 pF, load capacitance for all other outputs = 80 pF 8/	9,10,11	All	$2t_{CLCL-40}$		ns
Address valid to ALE low	t_{AVLL}				$t_{CLCL-40}$		
Address hold after ALE low	t_{LLAX}				$t_{CLCL-30}$		
ALE low to valid instruction in	t_{LLIV}					$4t_{CLCL-100}$	
ALE low to PSEN low	t_{LLPL}				$t_{CLCL-30}$		
PSEN pulse width	t_{PLPH}				$3t_{CLCL-45}$		
PSEN low to valid instruction in	t_{PLIV}					$3t_{CLCL-105}$	
Input instruction hold after PSEN	t_{PXIX}				0		
Input instruction float after PSEN	t_{PXIZ}					$t_{CLCL-25}$	
Address to valid instruction in	t_{AVIV}					$5t_{CLCL-105}$	
PSEN low to address float	t_{PLAZ}	Load capacitance for ____ port 0, ALE/PROG and PSEN = 100 pF, load capacitance for all other outputs = 80 pF 8/				10	
RD pulse width	t_{RLRH}				$6t_{CLCL-100}$		
WR pulse width ALE low	t_{WLWH}				$6t_{CLCL-100}$		
RD low to valid data in	t_{RLDV}					$6t_{CLCL-165}$	
Data hold after RD	t_{RHDX}				0		
DATA float after RD	t_{RHDZ}					$2t_{CLCL-60}$	
ALE low to valid data in	t_{LLDV}					$8t_{CLCL-150}$	
Address to valid data in	t_{AVDV}					$9t_{CLCL-165}$	
ALE low to RD or WR low	t_{LLWL}				$3t_{CLCL-50}$	$3t_{CLCL+50}$	
Address valid to WR low	t_{AVWL}				$4t_{CLCL-130}$		
Data valid before WR	t_{QVWX}				$t_{CLCL-50}$		
DATA hold after WR	t_{WHQX}				$t_{CLCL-50}$		
Data valid to WR high	t_{QVWH}				$7t_{CLCL-150}$		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.0\ V \le V_{CC} \le 6.0\ V$, $V_{SS} = 0.0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
RD low to address float	t_{RLAZ}	Load capacitance for port 0, ALE/PROG and PSEN = 100 pF, load capacitance for all other outputs = 80 pF 8/	9,10,11	All		0	ns
RD or WR high to ALE high	t_{WHLH}				$t_{CLCL-40}$	$t_{CLCL+40}$	
Serial port clock cycle time	t_{XLXL}	Serial port timing-shift register mode load capacitance = 80 pF			$12t_{CLCL}$		
Output data setup to clock rising edge	t_{QVXH}				$10t_{CLCL-133}$		
Output data hold after clock rising edge	t_{XHQX}				$2t_{CLCL-117}$		
Input data hold after clock rising edge	t_{XHDX}				0		
Clock rising edge to input data valid	t_{XHDV}					$10t_{CLCL-133}$	
Oscillator frequency	$1/t_{CLCL}$ 8/	External clock drive		01,03 02,04	3.5 3.5	12 16	MHz
High time	t_{CHCX}			All	20		ns
Low time	t_{CLCX}				20		
Rise time 2/	t_{CLCH}					20	
Fall time 2/	t_{CHCL}					20	

1/ The following pins are active low: INT0, INT1, WR, RD, EA of EA/V_{PP}, PROG of ALE/PROG, and PSEN. Case temperatures for devices 01, 02 are -55° C to +125° C, and for devices 03, 04 are -40° C to +85° C instant on. Unless otherwise specified, all test conditions shall be worst case condition. The supply voltage and operating temperature shall be as specifed in section 1.4.

2/ Guaranteed to the limits specified in table I, if not tested.

3/ Under steady state (nontransient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin:	10 mA
Maximum I_{OL} per 8-bit port - port 0	26 mA
Maximum I_{OL} per ports 1, 2 and 3	15 mA
Maximum total I_{OL} for all output pins:	71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed conditions.

4/ Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pFs, the noise pulse on the ALE signal may exceed 0.8 V. In these cases, it may be desirable to qualify ALE with schmitt trigger, or use an address latch with a schmitt trigger strobe input.

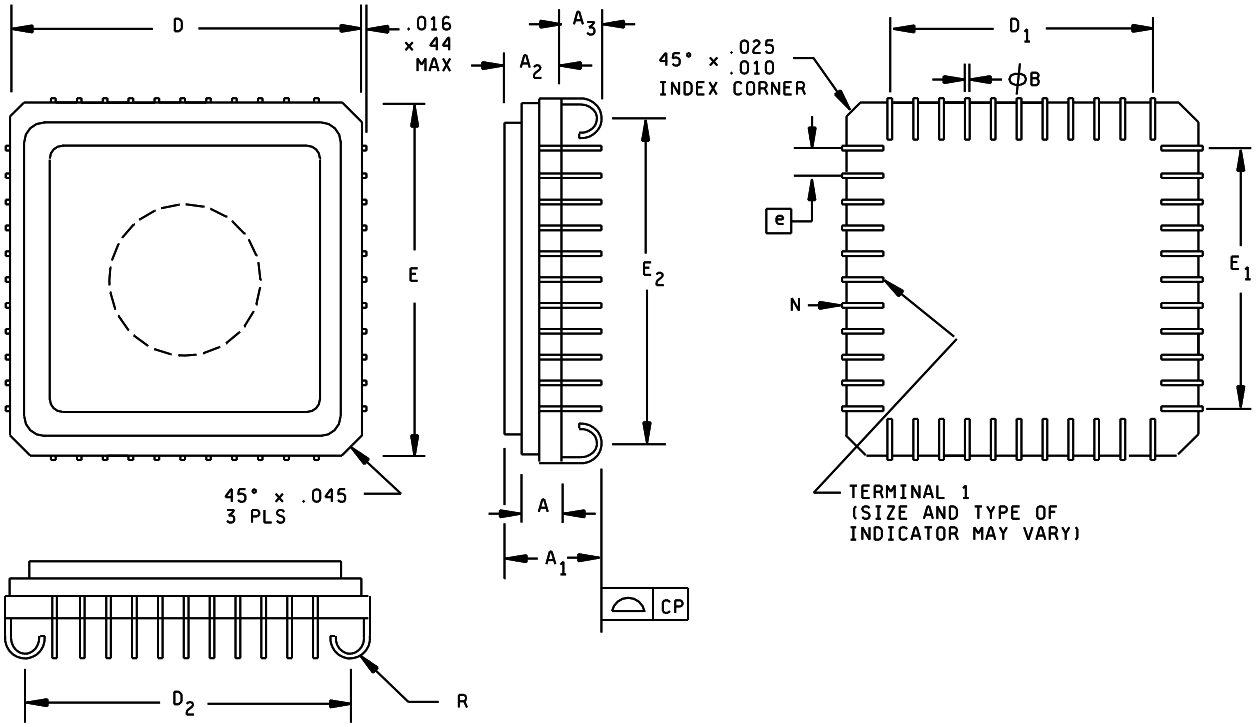
5/ Capacitive loading on ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the 0.9 V_{CC} specification when the address lines are stabilizing.

6/ Minimum V_{CC} for power down is 2.0 V.

7/ I_{CC} is measured with all output pins and XTAL2 disconnected; XTAL1 driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5\ V$, $V_{IH} = V_{CC} - 0.5\ V$ measured with EA and RST connected to V_{CC}. Idle and power down currents measured with EA and RST connected to V_{SS}. Power down currents measured with XTAL1 connected to V_{SS}.

8/ Timings tested at 16 MHz only but guaranteed across the specified operating frequency range

Case T



Ceramic chip carrier, "J" leaded package

FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216	SIZE A		5962-91697
		REVISION LEVEL B	SHEET 9

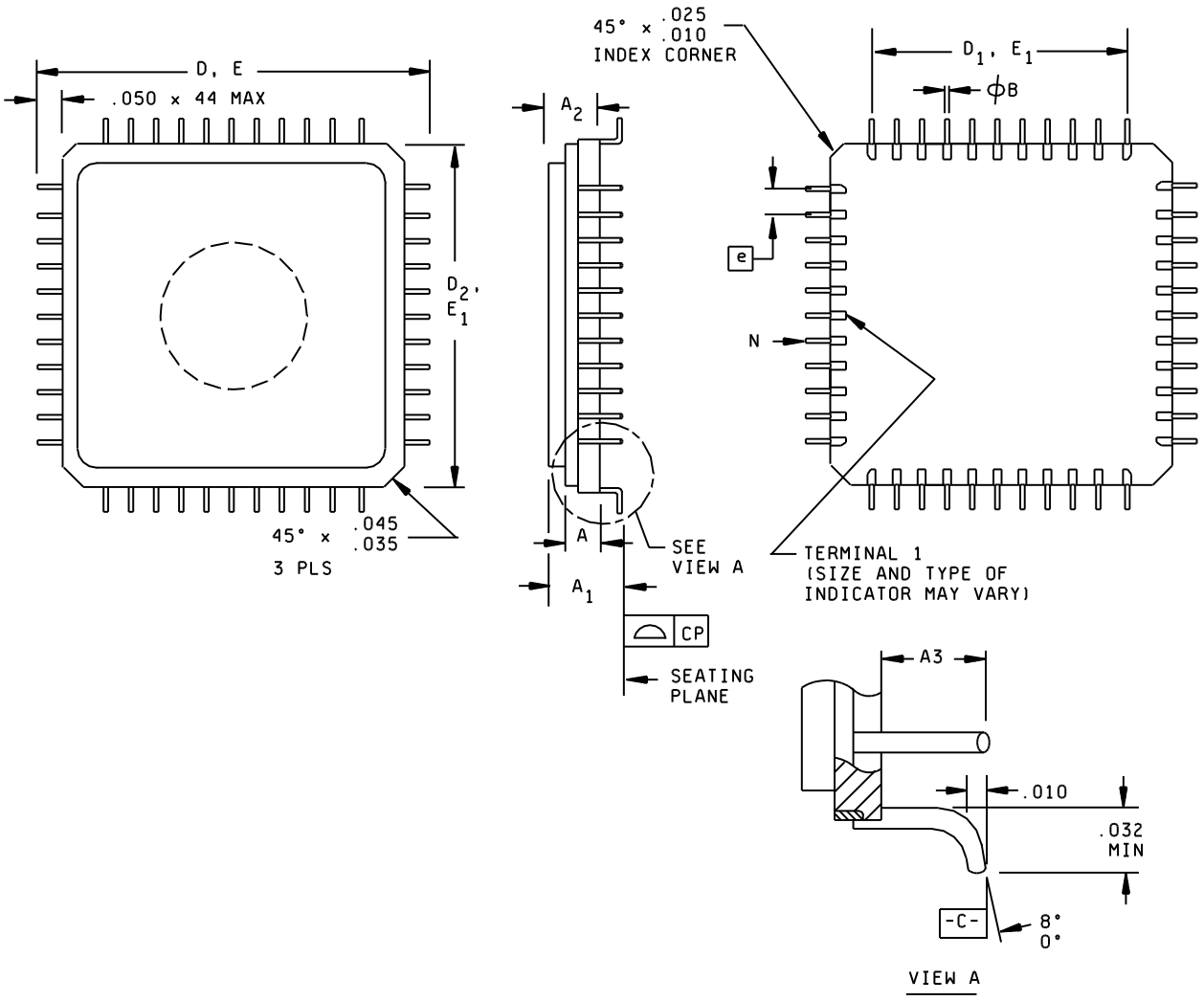
Case T

Family: Ceramic leadless chip carrier						
Symbol	Inches			Millimeters		
	Min	Max	notes	Min	Max	Notes
A	.060	.088		1.52	2.23	
A_1	.157	.200	EPROM lid	3.99	5.08	EPROM lid
A_2	.102	.134	EPROM lid	2.59	3.40	EPROM lid
A_3	.055	.065		1.40	1.65	
B	.014	.018		0.35	0.46	
CP	.000	.004		0.00	0.10	
D	.640	.670		16.25	17.02	
D_1	.500			12.70		
D_2	.600			15.24		
E	.640	.670		16.25	17.02	
E_1	.500			12.70		
E_2	.600			15.24		
e	.044	.056		1.12	1.42	
N	44			44		
R	.027	.033		0.69	0.84	

Ceramic chip carrier, J-leaded package

FIGURE 1. Case outlines - Continued.

Case Z



Ceramic chip carrier, gullwing-leaded package

FIGURE 1. Case outlines - Continued.

Case Z

Family: Ceramic leadless chip carrier						
Symbol	Inches			Millimeters		
	Min	Max	Notes	Min	Max	Notes
A	.060	.090		1.52	2.29	
A_1	.157	.200	EPROM lid	3.99	5.08	EPROM lid
A_2	.102	.134	EPROM lid	2.59	3.40	EPROM lid
A_3	.055	.065		1.40	1.65	
B	.014	.018		0.35	0.46	
CP	0.00	.004		0.00	0.10	
D	.716	.748		18.19	19.00	
D_1	.500			12.70		
D_2	.640	.660		16.25	16.76	
E	.716	.748		18.19	19.00	
E_1	.500			12.70		
E_2	.640	.660		16.25	16.76	
e	.044	.056		1.12	1.42	
N	44			44		

Ceramic chip carrier, gullwing-leaded package

FIGURE 1. Case outlines - Continued.

Case X, N

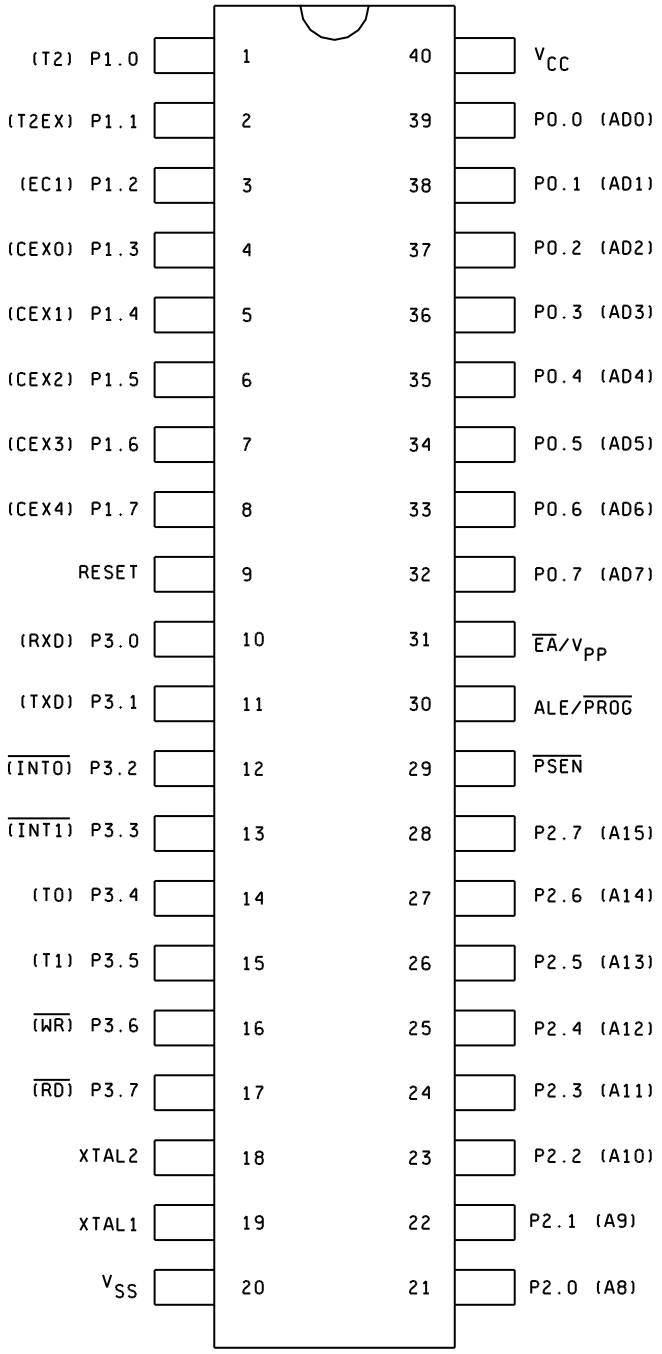


FIGURE 2. Terminal connections.

Case M, T, U, Y, and Z

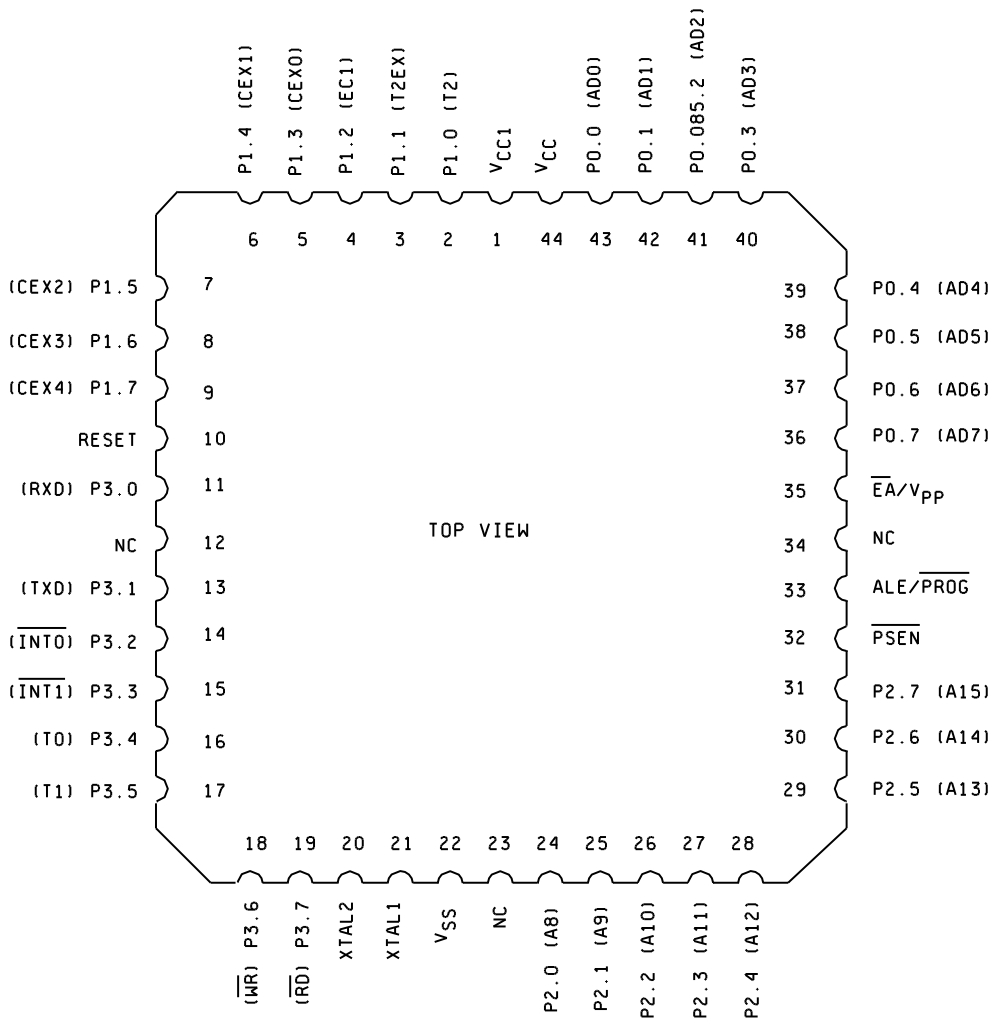
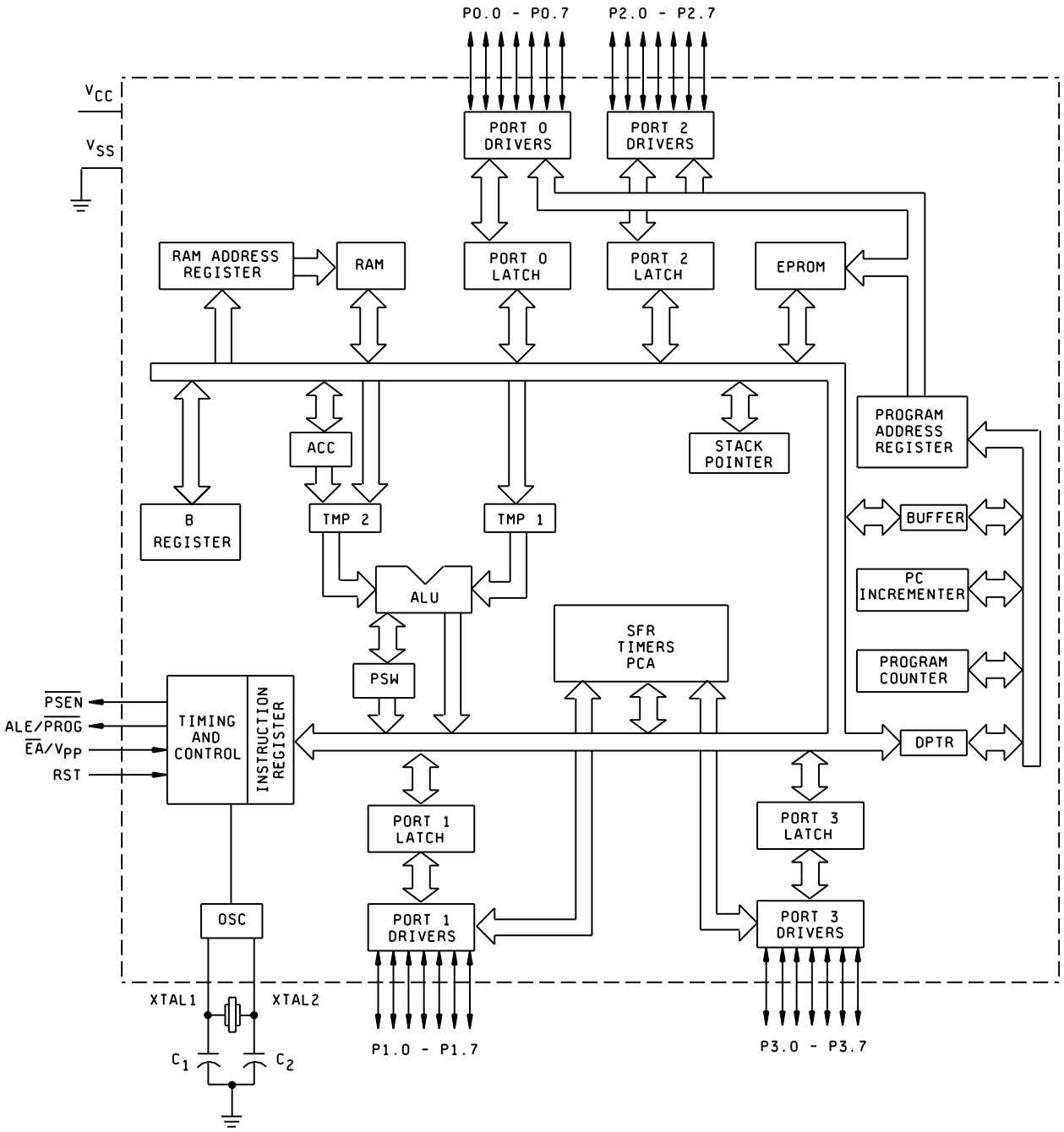


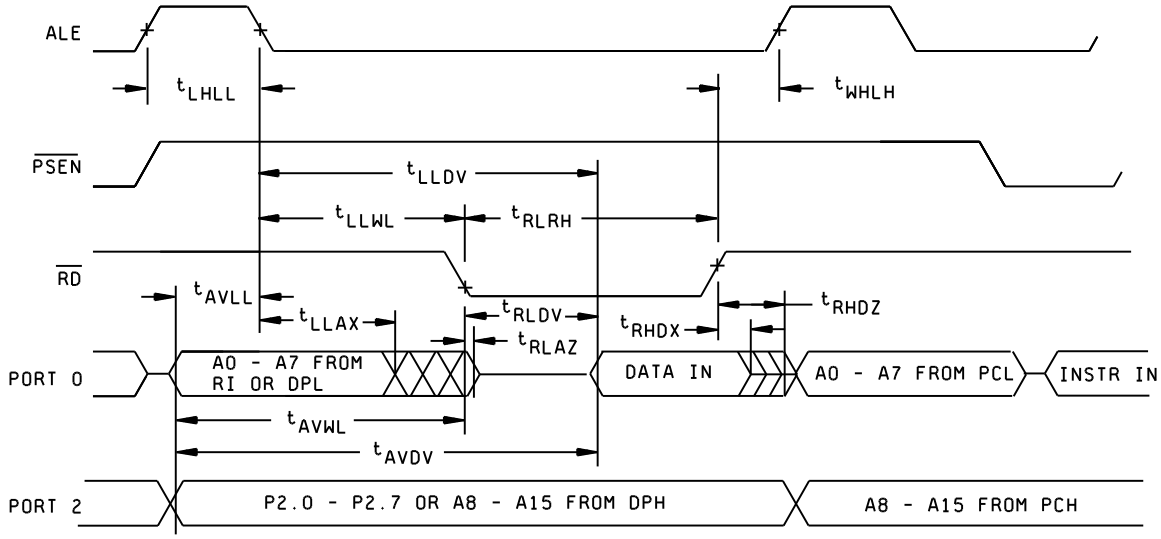
FIGURE 2. Terminal connections - Continued.



C_1, C_2 = 30 pF ± 10 pF for crystals.
C_1, C_2 = 10 pF for ceramic resonators.

FIGURE 3. Functional block diagram.

External data memory read cycle



External program memory read cycle

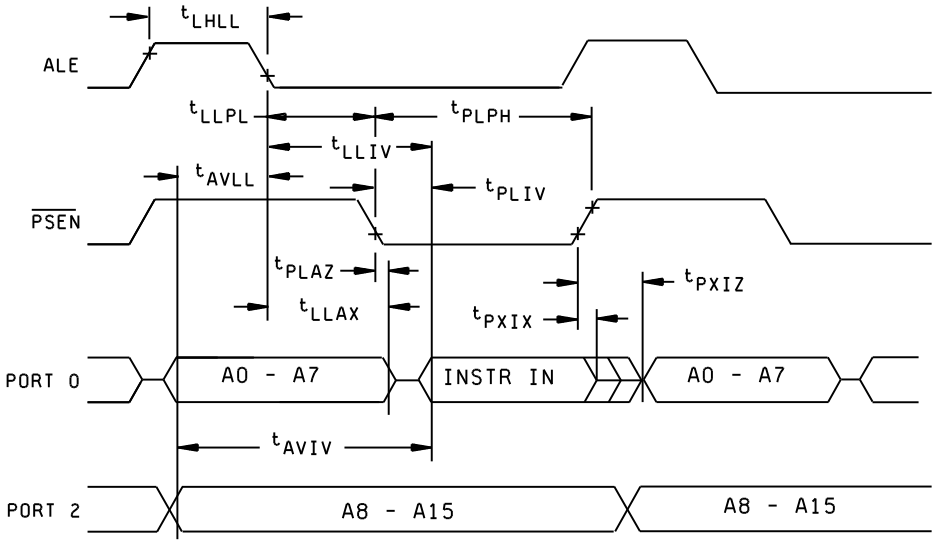
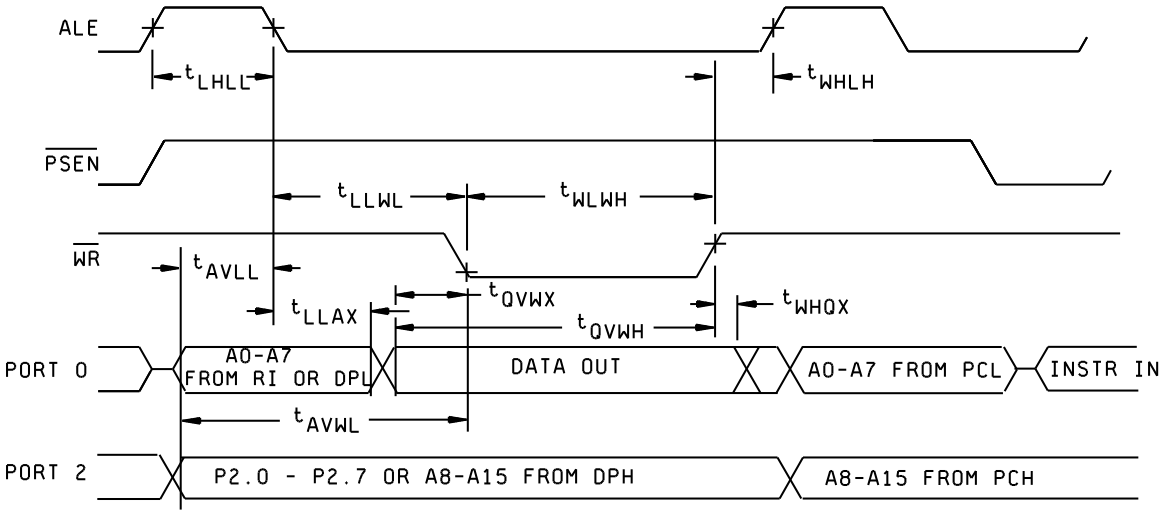


FIGURE 4. Switching waveforms and test circuit.

External data memory read cycle



External clock drive waveform

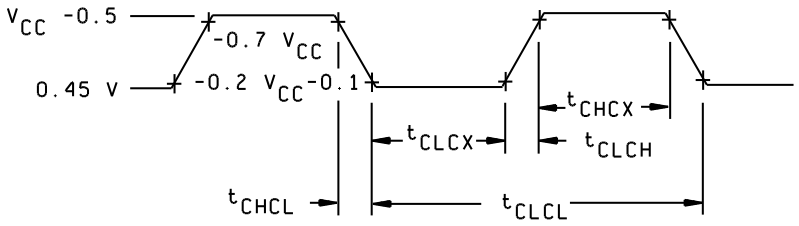
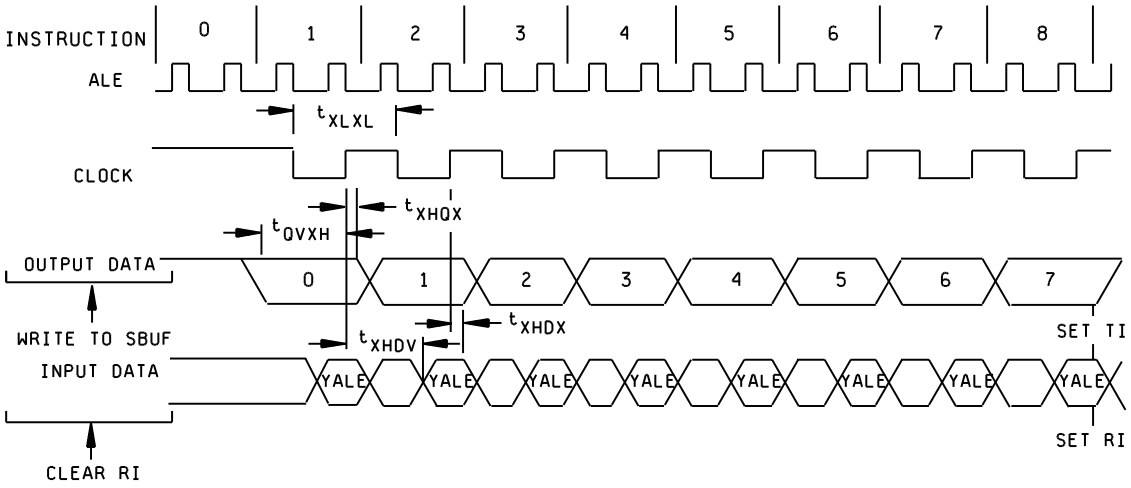


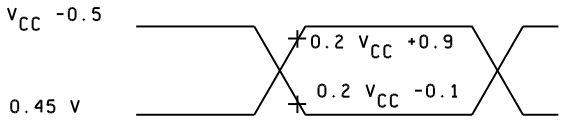
FIGURE 4. Switching waveforms and test circuit - Continued.

Shift register mode timing waveforms

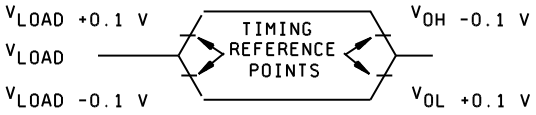


AC testing input

Input, output waveforms



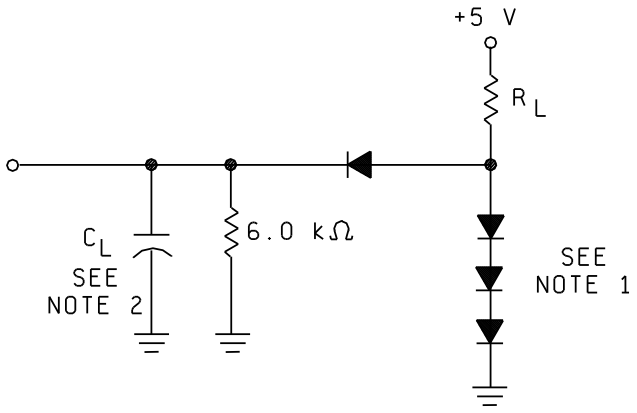
Float waveforms



AC inputs during testing are driven at V_{CC} -0.5 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at V_{IH} minimum for a logic "1" and V_{IL} maximum for a logic "0".

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH} / V_{OL} level occurs. I_{OL} / I_{OH} ≥ ± 20 mA.

FIGURE 4. Switching waveforms and test circuit - Continued.



Output	R_L	C_L
Port 0, ALE, PSEN	1.2 kΩ	100 pF
All other outputs	2.4 kΩ	80 pF

NOTES:
1. All diodes are 1N914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 4. Timing waveforms and test circuit -Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A. 1/

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.11.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_M = +5.9 V at +25°C using loose timing (i.e., T_{ACC} > 1 µs).

(4) Perform dynamic burn-in (see 4.2.1a).

(5) Margin at V_M = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.11.1), except devices submitted for groups A, B, C and D testing.

(8) Verify erasure (see 3.11.3).

Margin test method B. 2/

(1) Program at +25°C, 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C.

(3) Perform margin test at V_M = 5.9 V.

(4) Erase (see 3.11.1).

(5) Perform interim electrical tests in accordance with table II.

(6) Program 100 percent of the bits and verify (see 3.11.3).

(7) Perform burn-in (see 4.2a).

1/ Devices must have a transparent lid.
2/ For solid lid packages, steps 1-3 only.

(8) One-hundred percent test at +25°C (group A, subgroups 1 and 7). V_M = 5.9 V with loose timing, apply PDA.

(9) Perform remaining final electrical subgroups and group A testing.

(10) Erase, devices may be submitted for groups B, C, and D at this time.

(11) Verify erasure (see 3.11.3). Steps 1 through 4 are performed at wafer level.

4.2.2 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 5 and 6 in table I., method 5005 of MIL-STD883 shall be omitted

c. Subgroup 4 (C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified and the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available from the approved source of supply.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9,10, 11 1/	1,2,3,7,8,9,10, 11 1/	1,2,3,7,8,9,10, 11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,1 0,11	1,2,3,4,7,8,9,1 0,11	1,2,3,4,7,8,9,1 0,11
Group C end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group D end-point electrical parameters (see 4.4)	2,8A,10	2,8A,10	2,8A,10	2,8A,10
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25° C ±5° C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.6 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Connect the device in the electrical configuration (see figure 5) for programming. The waveforms of figure 5 and programming characteristics of table III shall apply.

b. Initially and after each erasure, all bits are in high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.5).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-EC, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

TABLE III. EPROM programming and verification characteristics.

Parameter	Symbol	Conditions	Limits		Unit
			Min	Max	
Programming supply voltage	V_{PP}	EPROM programming and verification characteristics See figure 5, T_A = 21° C to 27° C, V_{CC} = 5.0 V ± 0.25 V, V_{SS} = 0.0 V	12.5	13.0	V
Programming supply current	I_{PP}			75	mA
Oscillator frequency	$1/t_{CLCL}$		4	6	MHz
Address setup to PROG low 1/	t_{AVGL}		$48t_{CLCL}$		ns
Address hold after PROG 1/	t_{GHAX}		$48t_{CLCL}$		
DATA setup to $\overline{PROG}$ low 1/	t_{DVGL}		$48t_{CLCL}$		
Data hold after PROG 1/	t_{GHDX}		$48t_{CLCL}$		
P2.7 (enable) high to V_{PP} 1/	t_{ENSH}		$48t_{CLCL}$		ns
V_{PP} setup to $\overline{PROG}$ low 1/	t_{SHGL}		10		µs
V_{PP} hold after $\overline{PROG}$ 1/	t_{GHSL}		10		
$\overline{PROG}$ width 1/	t_{GLGH}		90	110	
Address to data valid 1/	t_{AVQV}			$48t_{CLCL}$	
Enable low to DATA valid 1/	t_{ELQV}			$48t_{CLCL}$	
DATA float after enable 1/	t_{EHQZ}		0	$48t_{CLCL}$	
$\overline{PROG}$ high to $\overline{PROG}$ low	t_{GHGL}		10		

1/ Guaranteed to the limits specified in table III, if not tested.

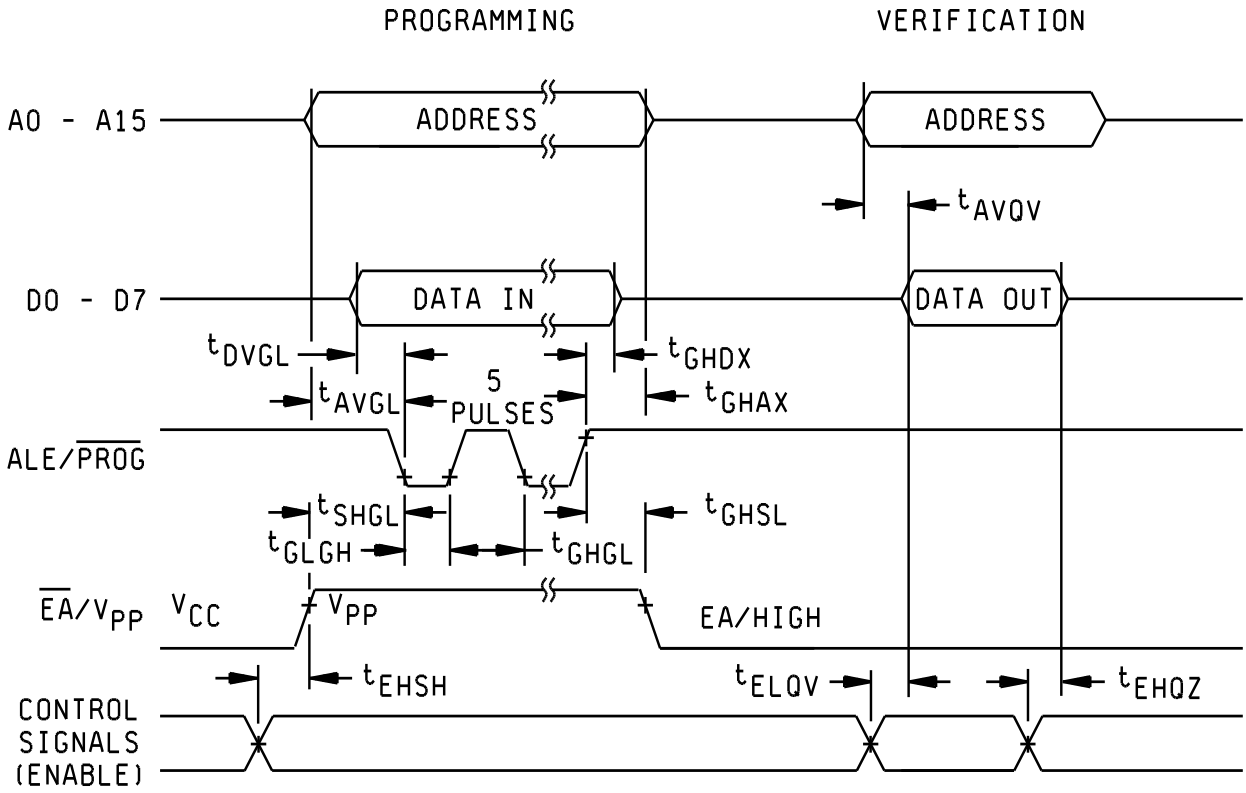


FIGURE 5. EPROM programming waveforms and configuration.

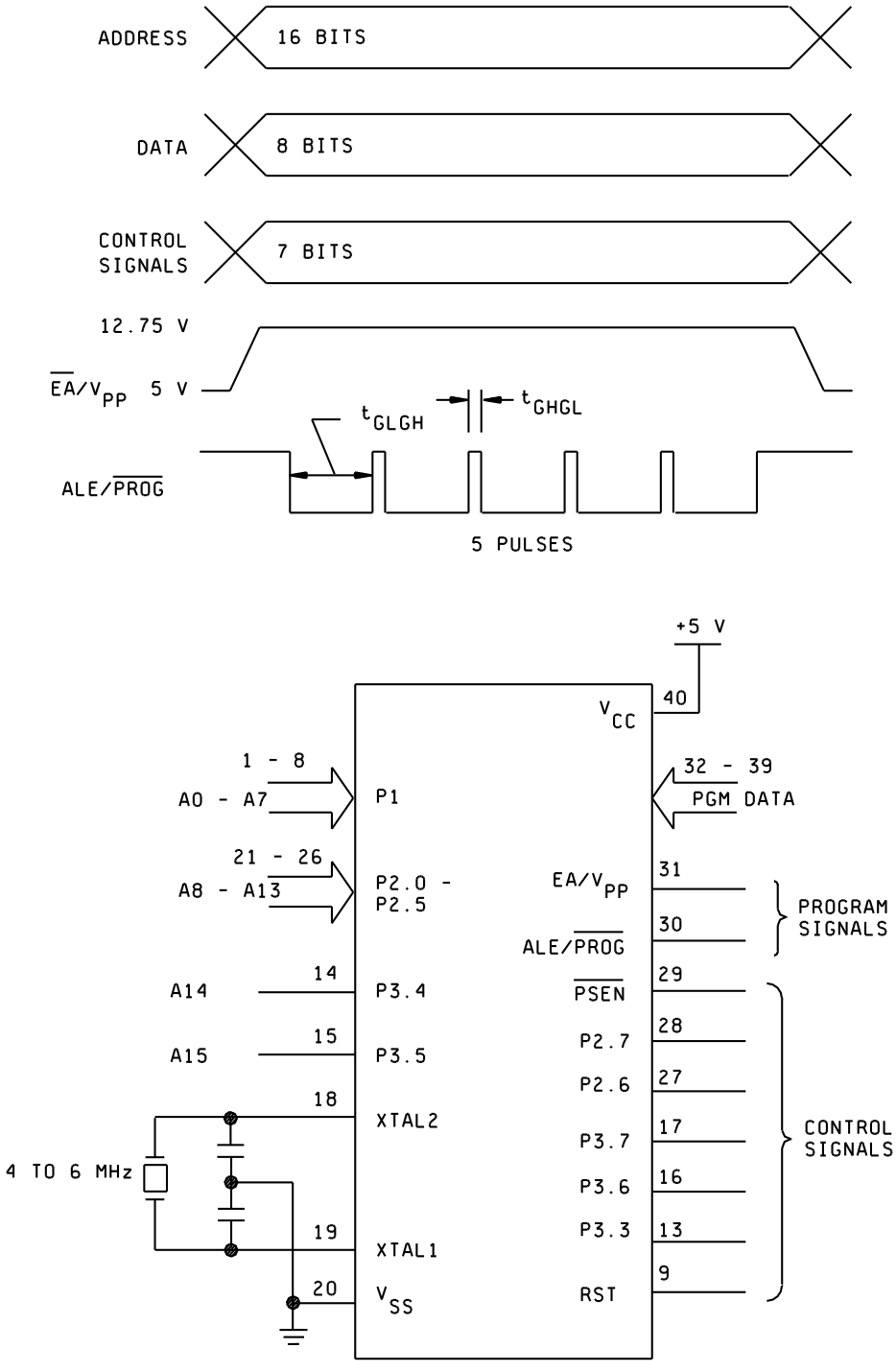


FIGURE 5. EPROM programming waveforms and configuration -Continued.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows.

Symbol	Definition	Functional description
BUS SIGNALS		
ABO-15	Address bus	Output used to indicate the memory address or I/O location. ABO is the most significant bit (MSB). These lines are three-state during cycles not assigned to the CPU. Recommended pull-up value: 1.0K Ω.
DBO-15	Data bus	A 16-bit bidirectional data bus used to transmit or receive data from the memory or I/O location. DBO is the most significant bit (MSB). These lines are three-state during bus cycles not assigned to the CPU. Recommended pull-up value: 4.7K Ω
BUS CONTROL		
D/$\overline{I}$	Data or instruction	An output signal that indicates whether the current bus cycle access is for Data (high) or for instruction (low). This signal is three-state during bus cycles not assigned to the CPU. Recommended pull-up value: 1K Ω
$\overline{M}$/IO	Memory or I/O	An output signal that indicates whether the current bus cycle is for memory (low) or I/O (high). This signal is three-state during bus cycles not assigned to the CPU. Recommended pull-up value: 1K Ω
R/$\overline{W}$	Read or write	An output signal that indicates whether the current bus cycle is a read (high) or write (low). This signal is three-state during bus cycles not assigned to the CPU. Recommened pull-up value: 1K Ω
$\overline{PSTRA}$	Physical strobe address	An active low output that can be used to externally latch the memory or XIO address at the low-to-high transition of the strobe. This signal is three-state during bus cycles not assigned to the CPU. Recommended pull-up value: 1K Ω
$\overline{STRD}$	Strobe data	A bidirectional signal. During bus cycles assigned to the CPU, STRD is an active low output that can be used to stobe data during memory or XIO cycles. Use the low-to-high transition to latch the data into memory or data buffers. During non-CPU bus cycles, STRD is an input and the trailing edge (low-to-high transition) is used for sampling bits into the fault Register. NOTE: This pin should never float. Recommended pull-up value: 1K Ω
$\overline{RDYD}$	Ready data	An active low input usually asserted by memory or I/O device to indicate the completion of a data cycle. When RDYD is not active, Wait states are inserted by the CPU. This will stretch out the bus cycle until RDYD is active. Adds S3 states on reads and S4 states on writes. Recommended pull-up value: 1K Ω

Symbol	Definition	Functional description
BUS ARBITRATION		
$\overline{\text{BGNT}}$	Bus grant	An active low input from an external arbiter that indicates the CPU may use the bus.
$\overline{\text{BREQ}}$	Bus request	An active low output indicates the CPU is ready to execute a bus cycle. During internal CPU cycles, this output is inactive (high).
$\overline{\text{BSYI}}$	Busy in	An active low input indicates to the CPU that the bus is currently in use.
BSYO	Busy out	An active high output indicates that the CPU is currently using the bus. NOTE: During the execution of the TSB instruction, the bus will remain "locked" until the completion of the instruction. The BSYO signal will remain high until the completion of the instruction.
CLOCK		
CLK	CPU Clock	Input clock signal (square wave, 40% to 60% duty cycle).
TCLK	Timer clock	A 100 KHz square wave clock input used for timers A and B.
EXTERNAL REQUEST		
$\overline{\text{RST}}$	Reset	A synchronous active low input that initializes the CPU in accordance with MIL-STD-1750A. The initialization is executed after the completion of the current internal CPU cycle.
$\overline{\text{PNLR}}$	Panel request	An active low input that causes the CPU to HALT at the end of the current instruction and to enter into the panel mode. The CPU will then execute an I/O cycle to read the panel command from the data bus.
$\overline{\text{PRST}}$	Power up reset	An asynchronous active low input that initializes the CPU in accordance with MIL-STD-1750A. This signal should only be used during the power-up sequence, as there is a chance to write bad data to memory or I/O.
$\overline{\text{STC}}$	Stop counters	An active low input that inhibits the counting of timers A and B.
$\overline{\text{HLDEN}}$	Hold enable	An active low input that enables the CPU to respond to the PNLR input. NOTE: If HLDEN is low, the BPT instruction will place the CPU in HALT mode allowing for panel operations. When HLDEN is high, the BPT instruction is treated as a NOP. This signal should not be used to exit the panel mode.

Symbol	Definition	Functional description
EXTERNAL REQUEST - Continued.		
Wait	Wait	An active high input extends the bus cycle. Wait operates similarly to Ready data but with the opposite sense. When wait is low, the extra wait states are added (S3 on reads and S4 on writes). The wait signal must be high to avoid the wait states. Wait has priority over ready data.
$\overline{\text{DMAC}}$	DMA Cycle	An active low input asserted by an external bus arbiter indicating that the bus is currently granted to the DMA device. This signal is used by the CPU to enable the sampling of the DMA faults.
FAULTS		
$\overline{\text{UAER}}$	Unimplemented Address error	An active low input sampled by the fault register at the end of each bus cycle asserted by the CPU. If UAER is low during the memory cycle, bit 8 is set. If it is low during the I/O cycle, bit 5 is set.
$\overline{\text{PAER}}$	Parity error	An active low input sampled by the fault register at the end of each CPU bus cycle. If PAER is low during the memory cycle, bit 2 is set. In the DMA cycle (DMAC is low), the PAER is sampled by the STRD signal and bit 4 is set.
$\overline{\text{MPER}}$	Memory Protect error	An active low input sampled by the fault register at the end of each CPU bus cycle. If low during the memory cycle asserted by the CPU, bit 0 is set at the end of CPU cycle. In DMA cycle (DMAC is low), MPER is sampled by the STRD signal and bit 1 is set. NOTE: This input is generated by the MMU or BPU of the MBU chip to indicate that an access fault, execute protect, or write protect violation has been detected.
SPRF0/1	Spare faults	These signals are asynchronous fault inputs that are active on the high-to-low transition. When active, bit 15 or 7 of the fault register is set.
$\overline{\text{PTF}}$	Programmed I/O Trans-mission fault	An active low input sampled by the fault register at the end of each bus cycle asserted by the CPU. When active low, bit 6 is set.
INTERRUPTS		
PFINT	Power fail interrupt	The high-to-low transition of this input sets an internal flip-flop which is sensed on the next S0 CLK cycle. This sets bit 0 of the pending Interrupt register, making it the highest priority interrupt, and cannot be disabled or masked.

Symbol	Definition	Functional description
INTERRUPTS - Continued.		
UINT-2 UINT-8 UINT-10 UINT-11 UINT-13 UINT-15	User interrupts	Six user-defined interrupts with priority 2, 8, 10, 11, 13, and 15, respectively. On the high-to-low transition, they set internal flip-flops and are sensed on the next clock cycle. They can all be masked and disabled.
$\overline{\text{IOLINT1}}$ $\overline{\text{IOLINT2}}$	I/O Levels	Two active low signals which correspond to interrupt priority levels 12 and 14 as specified in MIL-STD-1750A. The low level is sensed at the rising edge of the next clock. Both can be masked and disabled. NOTE: These inputs are level interrupts and should be removed with the INTA signal.
SPECIAL SIGNALS		
HLDAK	Hold Acknowledge	An active high output indicates the CPU is in PANEL HOLD mode. The CPU enters this mode only if the HLDEN input is lowlow and the BPT instruction is fetched, or if the HLDEN is low and the PNLR input was initiated.
$\overline{\text{PWRUP}}$	Power up	An active LOW output that indicates that the CPU has successfully completed the built-in test and is initialized to MIL-STD 1750. The built-in test checks chip timing, microcode sequencer, and basic registers.
$\overline{\text{INTA}}$	Interrupt acknowledge	An active low output that occurs during the sixteenth bus cycle of the Interrupt request routine sequence. This signal is used in conjunction with XIO 1000h to inform the interrupting device that its interrupt is being serviced by the CPU. The interrupts are then disabled. This output can be used with the appropriate data bit to reset the acknowledged interrupt.
$\overline{\text{SNI}}$	Start new instructions	The low-to-high transition indicates that a new instruction will start execution on the next bus cycle. The high-to-low transition indicates that this is the start of the last machine cycle for the current instruction. The signal will remain low during the instruction fetch or if the CPU is executing a series of single machine cycle instructions.
$\overline{\text{EDOBF}}$	Enable data Output buffer	An output that indicates the direction of the data on the data bus. When low, the data is going out of the CPU. When high, data is coming into the CPU. This signal can be used to enable an external output buffer to the bus system.
$\overline{\text{ENOB}}$	Enable output buffer	An active low output that is used to enable the external output buffers for the address lines and bus control signals.

Symbol	Definition	Functional description
SPECIAL SIGNALS - Continued.		
$\overline{\text{MERR}}$	Machine error	An active low output signal that indicates that one or more bits in the fault register are set. This signal is also used internally by the CPU to set bit 1 of the pending interrupt register to indicate the machine error. The CPU will then process the interrupt if it is not masked.
$\overline{\text{IXRD}}$	Internal XIO ready	An active low output that indicates that one of the internally implemented XIO is being executed. This signal should be ANDed with the externally generated ready data signal to form the RDYD input signal.
INTSTF	Interrupt status flag	An output indicating the status of the interrupt mechanism. A high indicates enable and a low indicates disable status. This signal is useful in the debugging phase of the user's software.
CP	Clock Pulse	An output used for debugging. On a low-to-high transition, this output (the S0 bus cycle) indicates the beginning of an internal CPU cycle. If RDYD is not activated or the Wait signal is asserted, the low state of the CP signal is extended.
MBU FUNCTION		
$\overline{\text{MBRDY}}$	MBU Ready	An active low input from the MBU chip. This signal indicates that the MBU has completed the logical-to-physical address translation. If the MBU is not used, this input should be connected to GND.
$\overline{\text{MBC}}$	MBU Connected	When the MBU chip is used, this pin should be connected to GND. If the MBU chip is not used, connect the pin to V_{DD}.
MBA3 MBA2 MBA1 MBA0	MBU Address	Four output signals used by the MBU chip. These signals are the same as ABO-3, but occur one clock cycle earlier and do not have three-state buffers. If the MBU chip is not used, these signals should not be connected.
$\overline{\text{LSTRA}}$	Logical Strobe Address	An active low output used only by the MMU (in the MBU chip) to latch the logical memory address. When the MBU is used, this signal should be pulled-up with a 1.0K Ω resistor. If the MBU chip is not used, this signal should not be connected.

Symbol	Definition	Functional description
MBU FUNCTION - Continued.		
MBDI	MBU Data or instruction	An output signal used by the MBU chip. This signal is the same as D/I but one clock cycle earlier and without a three-state buffer. If the MBU chip is not used, this signal should not be connected.
MBM	MBU Memory	An output signal used by the MBU chip. This signal is the same as M/IO but occurs one cycle earlier and without three-state buffer. If the MBU chip is not used, this signal should not be connected.
MBS	MBU Status	An active low pulse used by the MBU. This signal indicates that the status register has been changed. If the MBU chip is not used, this signal should not be connected.
AS3 AS2 AS1 AS0	Address state	Four output signals used by the MBU chip to select the page register in the MMU. These outputs are three-state during bus cycles not assigned to the CPU and require pull-up resistors (recommended value: 4.7K Ω).
AK3 AK2 AK1 AK0	Access key	Four output signals used by the MBU to match the Access Lock. These outputs are three-state during bus cycles not assigned to the CPU and require pull-up resistors (recommended value: 4.7K Ω).
TEST FUNCTION (factory use)		
TST1	Test 1	This input is used for factory testing. This input must be connected to VDD.
$\overline{\text{TST2}}$	Test 2	This input is used for factory testing. This input must be connected to GND.
TST01 TST02	Test outputs	These two outputs are for factory testing. USERS SHOULD NOT CONNECT THESE PINS.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-09-03

Approved sources of supply for SMD 5962-91697 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9169701MTA	34649	MT87C51FC
5962-9169701MUA	34649	MR87C51FC
5962-9169701MXA	34649	MD87C51FC
5962-9169701MZA	34649	MZ87C51FC
5962-9169701NNA	18324	87C51FC/CN40A
5962-9169701NYA	18324	87C51FC/CA44A
5962-9169702MTA	34649	MT87C51FC-16
5962-9169702MUA	34649	MR87C51FC-16
5962-9169702MXA	34649	MD87C51FC-16
5962-9169702MZA	34649	MZ87C51FC-16
5962-9169702NNA	18324	87C51FC-16/CN40A
5962-9169702NYA	18324	87C51FC-16/CA44A
5962-9169703NNA	18324	87C51FC/IN40A
5962-9169703NYA	18324	87C51FC/IA44A
5962-9169704NNA	18324	87C51FC-16/IN40A
5962-9169704NYA	18324	87C51FC-16/IA44A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 3065 Bowers Avenue. Santa Clara Ca 95051 Point of contact: 5000 W. Chandler Blvd. Chandler AZ 85226
18324	Philips Semiconductor, Incorporated 811 East Arques Avenue Sunnyvale, CA 94086